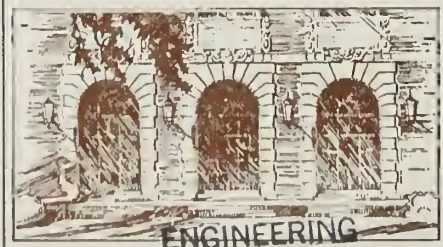


LIBRARY OF THE
UNIVERSITY OF ILLINOIS
AT URBANA-CHAMPAIGN

510.84

Il63c

no. 21-30



AUG 5 1976

The person charging this material is responsible for its return to the library from which it was withdrawn on or before the **Latest Date** stamped below.

Theft, mutilation, and underlining of books are reasons for disciplinary action and may result in dismissal from the University.

UNIVERSITY OF ILLINOIS LIBRARY AT URBANA-CHAMPAIGN

APR
APR

8 1980

ENGINEERING

CONFERENCE ROOM

JUL 1 1980

JUN 12 RECD

DEC 15 RECD

510.84
I463c
no.27

Engin.

ENGINEERING LIBRARY
UNIVERSITY OF ILLINOIS
URBANA, ILLINOIS

CONFERENCE ROOM

Center for Advanced Computation

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN
URBANA, ILLINOIS 61801

CAC Document No. 27

THE APPLICATION OF PLASMA PANEL
TECHNOLOGY TO GRAPHIC DISPLAY TERMINALS

By

Michael L. McMahan

January 7, 1972

CAC Document No. 27

THE APPLICATION OF PLASMA PANEL
TECHNOLOGY TO GRAPHIC DISPLAY TERMINALS

By

Michael L. McMahan

Center for Advanced Computation
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801

January 7, 1972



Digitized by the Internet Archive
in 2012 with funding from
University of Illinois Urbana-Champaign

<http://archive.org/details/applicationofpla00mcma>

Acknowledgements

I wish to express my thanks to Jack Stifle whose work on the PLATO IV Plasma Display Terminal contributed greatly to this paper and especially to Roger Johnson for his time and the many helpful comments and suggestions which made this effort possible.

Table of Contents

Introduction	1
1.0 Plasma Display Technology	3
1.1 Panel Structure	3
1.2 Panel Operation	3
1.2.1 Drive/Addressing Techniques	8
1.2.2 Full Screen Erasure	10
1.2.3 Electrical Readout	14
1.3 Display Effectiveness Factors	17
1.4 Research and Commercial Availability	19
2.0 Model Development	21
2.1 Model Description	23
2.1.1 Panel	23
2.1.2 Communication Lines	24
2.1.2.1 Control Lines	24
2.1.2.2 Serial Data Lines	25
2.1.2.3 Parallel Data Lines	26
2.1.2.4 Output Lines	26
2.1.3 Visual Output	27
2.2 Four Illustrative Models	28
2.2.1 Full Serial	28
2.2.2 Full Parallel	30
2.2.3 Full Serial With Readout	32
2.2.4 Semi-Parallel With Readout	32
3.0 Overview	36
3.1 Terminal Design	36
3.1.1 PLATO IV Terminal	38
3.1.2 Modification of Basic Terminal	39

Table of Contents
(Cont.)

3.2	User-Oriented Capabilities	42
3.3	Conclusions and Recommendations	44

References

List of Figures

Number	Description	Page
1-1	Panel Structure	4
1-2	Display Element Bistability	6
1-3	Applied Voltage vs V_w	7
1-4	State Transitions	7
1-5	Drive Circuit Schematic	9
1-6a	Parallel Addressing	11
1-6b	Serial Addressing	12
1-6c	Semi-Parallel Addressing	13
1-7	Lumped Parameter Element Model	15
1-8	Sensing Circuit	15
1-9a	Serial Readout	16
1-9b	Parallel Readout	16
2-1	Model—Block Diagram	22
2-2a	Model I	29
2-2b	Model I—Input Word	29
2-3a	Model II	31
2-3b	Model II—Input Word	31
2-4a	Model III	33
2-4b	Model III—Input Word	33
2-5a	Model IV	34
2-5b	Model IV—Input Word	34
3-1	PLATO IV Terminal—Modified Block Diag.	37
3-2	Modified Terminals—Block Diag.	40

Introduction

The introduction of the plasma display in the mid-1960's promised the advent of relatively inexpensive computer graphics. Only recently, however, has this technology become commercially available. Since the Center for Advanced Computation is now anticipating the installation of an on-site computer system and is also interested in display terminals to be used on the ARPA net, it will be a valuable exercise to examine the current feasibility of using plasma displays in these applications.

This technology has a number of characteristics which make it extremely attractive. Foremost is the fact that the plasma display/memory unit exhibits inherent memory and consequently does not require an expensive local memory to "hold up" the display image, thus eliminating "flicker." Since the panel itself is flat, and its thickness (about $\frac{1}{2}$ ") is largely independent of screen size, it is not limited to typical CRT installations, but it may be used on walls, desks, etc. . A particularly intriguing possibility involves the use of plasma panels in large screen group displays (1). Finally, since the panel is actually transparent, it lends itself to the rear-projection of micro-film, slides, maps, etc. which are superimposed on the dynamic computer-generated graphics.

This paper will be divided into three sections. The first will cover the basics of plasma display technology, describing panel operation, input/output techniques, and display characteristics. Section II will develop a model of the display module which will be used to describe a family of possible plasma display/memory units. Finally, various

terminal design options will be discussed, drawing heavily on Section II and the PLATO IV terminal design. This last section will concentrate on user-oriented terminal operating capabilities, discussed as a function of the design options described earlier.

1.0 Plasma Display Technology

1.1 Panel Structure

The plasma display/memory panel is constructed with two parallel sheets of glass encompassing a narrow, gas-filled gap (Fig. 1-1). Early panels also had a third center sheet, perforated with an array of holes to define the gas discharge cells. Present versions use the "open cell" technique in which the "intersection" of two orthogonal sets of electrodes, deposited on the two glass surfaces, define the array of light-emitting elements (11).

1.2 Panel Operation

In its most basic form each gas discharge cell acts as a bistable device. The "0" or "OFF" state is characterized by the absence of a discharge sequence in the gas and therefore the absence of any emitted light. The "1" or "ON" state is defined by the presence of pulsed discharges and corresponding light outputs. The mathematical details of the operation of these bistable elements has been described elsewhere (12). This discussion will simply attempt to provide enough background material to facilitate an understanding of the panel's operation and application as a display device.

Each discharge cell is excited by an AC sustaining voltage, $V_s(t)$. The voltage which actually appears across the gap, however, is

$$V_G(t) = K \cdot V_s(t) + V_w(t)$$

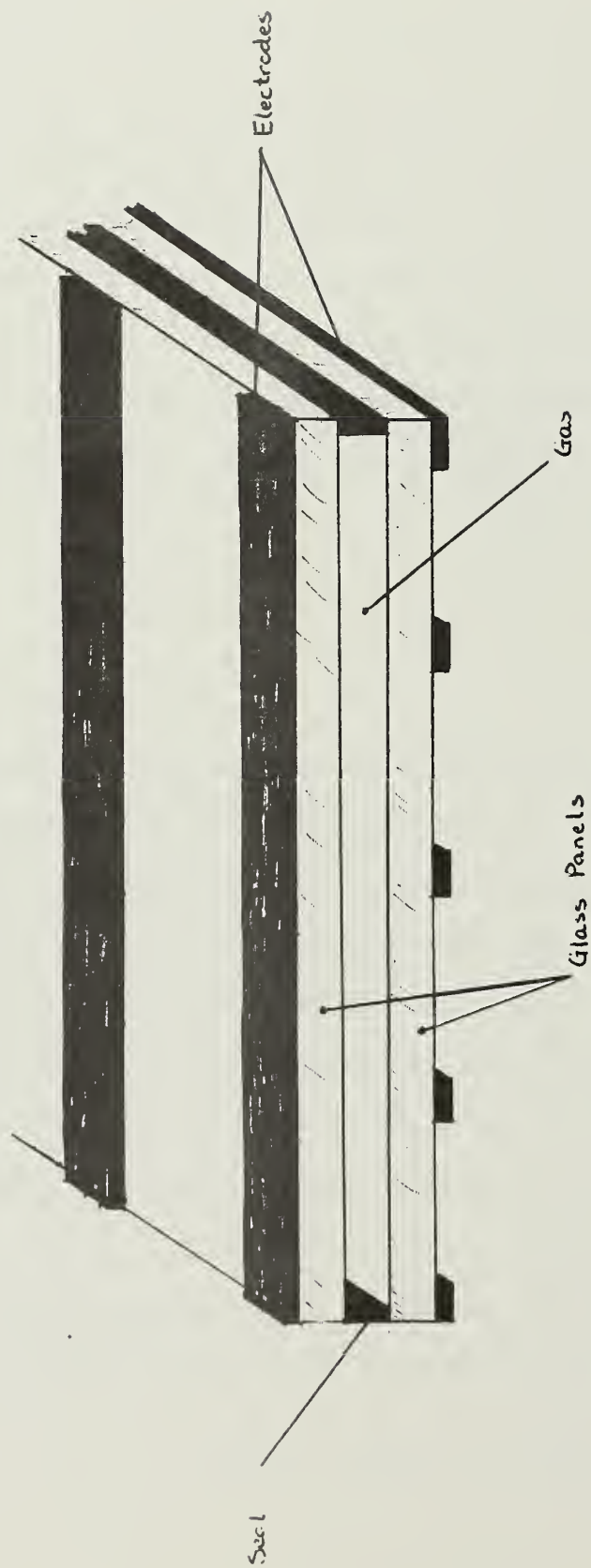


Fig. 1-1
Panel Structure

$V_w(t)$ represents the wall voltage due to charge built up on the dielectric walls during a previous discharge, while K stands for the fraction of the sustaining voltage which actually appears across the gap. The latter is adjusted so that alone, it is insufficient to trigger breakdown. If, however, there exists a residual wall voltage such that

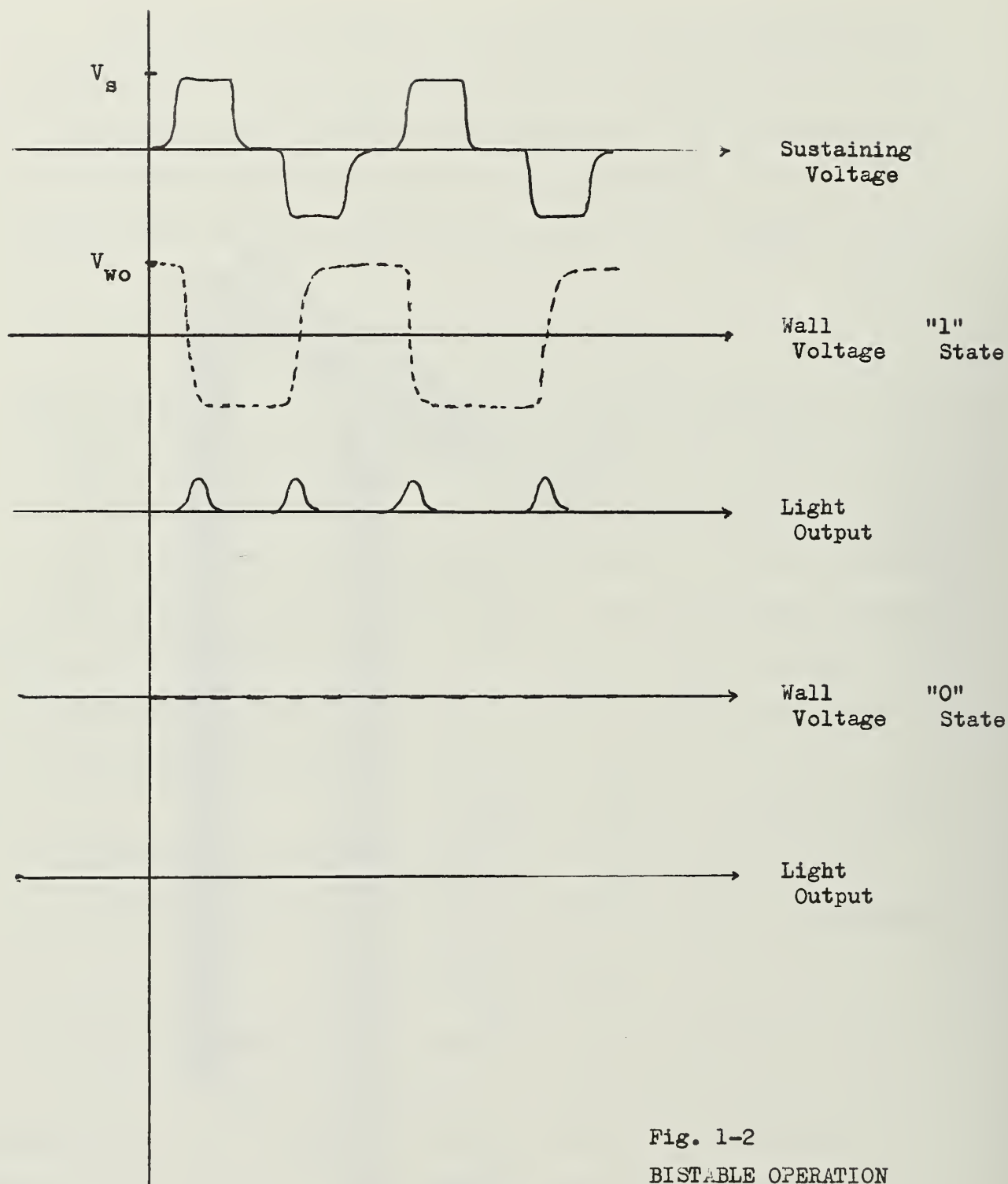
$$V_G(t) = K \cdot V_s(t) + V_{wo} > V_f$$

(V_f = the breakdown voltage of the gas in the gap). Ionization of the gas will follow. The resulting currents in the gap during this time build up charge on the cell walls tending to counteract the applied voltage until the discharge is extinguished; $V_w(t)$ now equals $-V_{wo}$. When the sustaining voltage reverses polarity, $V_s(t)$ and $V_w(t)$ again add to exceed V_f and the process is repeated. Discharges (light pulses) will therefore occur twice during every cycle of the sustaining waveform (Fig. 1-2). Stability criteria for such discharge series have been described by Slottow and Petty (4).

Control of the state of individual elements can be achieved by superimposing a second applied voltage, $V_p(t)$, on $V_s(t)$ such that

$$K \cdot (V_s(t) + V_p(t)) > V_f$$

If $V_p(t)$ is chosen so that the change in wall voltage will be exactly V_{wo} (Fig. 1-3), it will force a state transition from "1" to "0" or vice versa (Fig. 1-4). Since a plasma panel is made up of a rectangular array of elements, the control voltage is actually used in two components, V_x and V_y , in a coincident addressing scheme. If chosen properly, neither V_x or V_y alone will be sufficient to cause breakdown (Fig. 1-3).



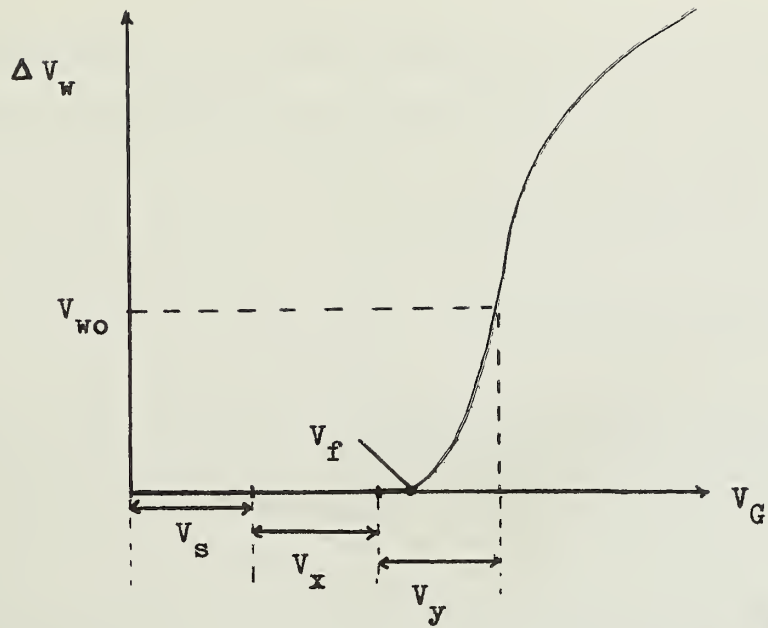


Fig. 1-3
APPLIED VOLTAGE
MAGNITUDES

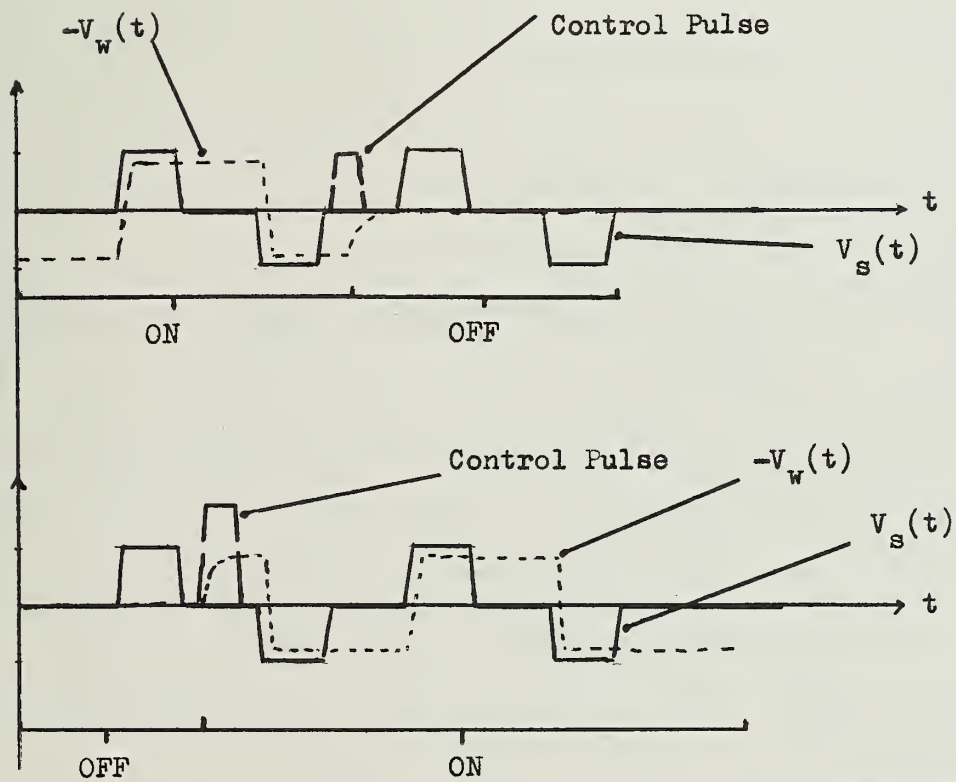


Fig. 1-4
STATE TRANSITION

Only at the intersection of the chosen axes will a state transition occur. This is the basis of the random access (write or erase) property of the plasma panel.

1.2.1 Drive/Addressing Techniques

The coincident addressing property of plasma panels lends itself to use in two extreme data transfer techniques, bit or word oriented input/output.

The simplest addressing scheme is to use a drive circuit on each X and each Y line (Fig. 1-5 illustrates basic drive circuit schematic). Each line could then be driven independently, and words up to the screen width in length could be addressed during one operation. The disadvantage of this parallel method is the cost of supplying many separate drive components. Assuming a panel arranged in a $M \times N$ matrix, the cost would be proportional to $M+N$: $C_P = C_O \cdot (M + N)$.

To avoid this excessive expense a second addressing method is commonly used. This technique involves dividing the lines along each axis into "orthogonal sets." By driving one group of lines from each set, a single row and column will be accessed, defining a unique address at their intersection. The obvious advantage of this multiplexing technique is a reduction in the number of drive circuits required. In general, $C_S = C_O \cdot (\sqrt{M} + \sqrt{N})$. Unfortunately the units flexibility is reduced, since it is now limited to serial inputs.

A third technique which combines some of the advantages of both extremes is presently being developed at Owens-Illinois. This method

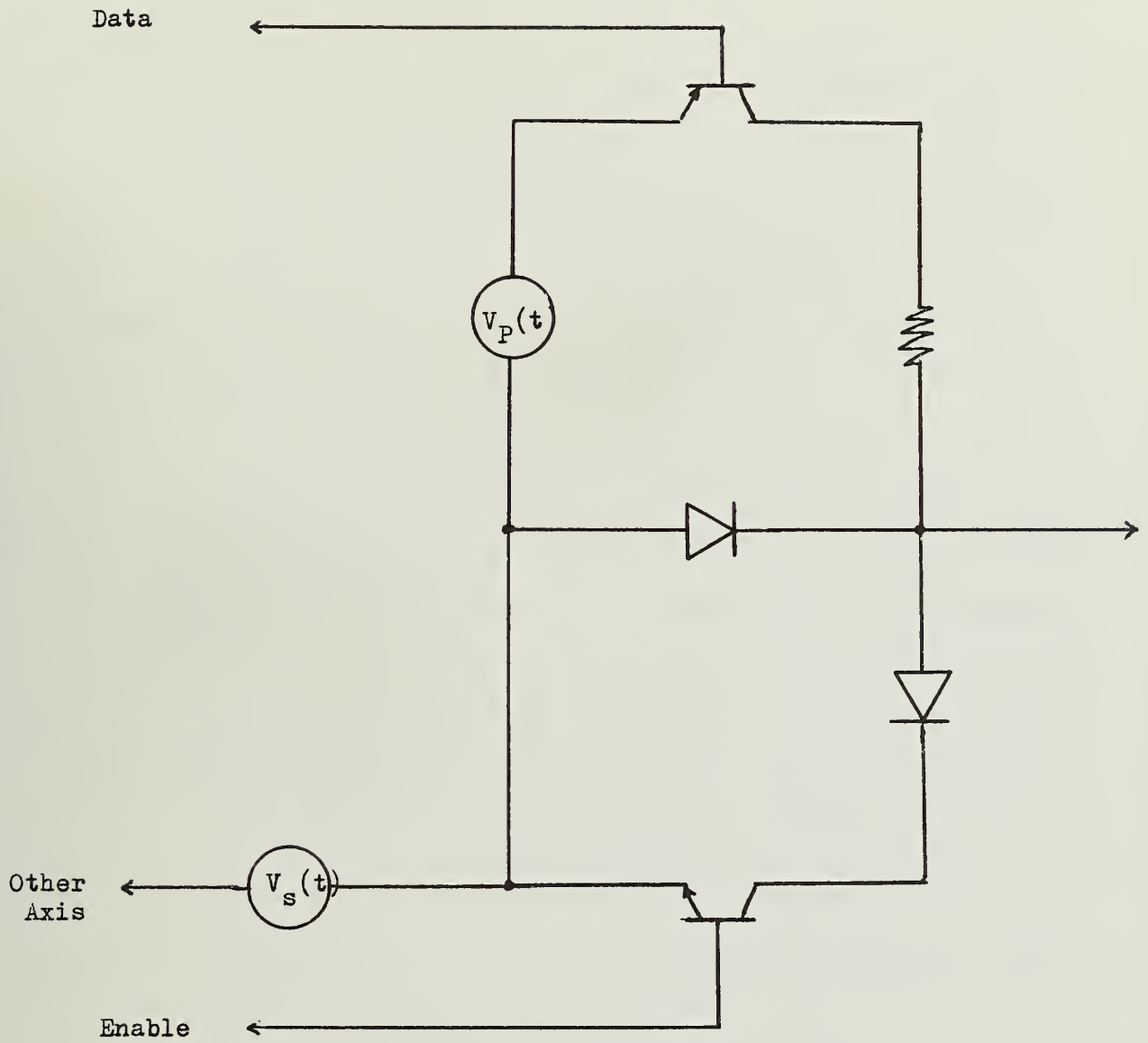


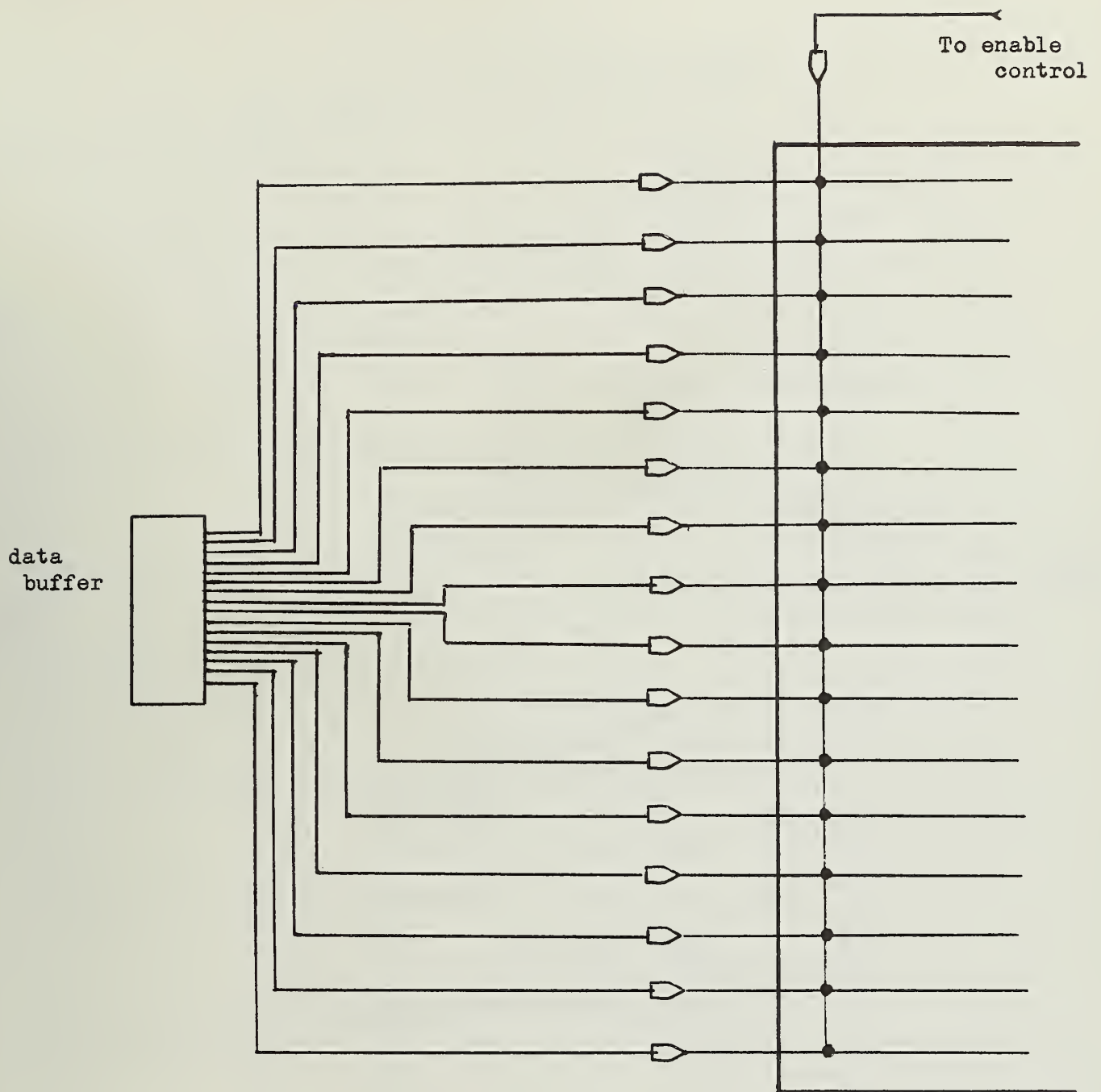
Fig. 1-5

DRIVE CIRCUIT SCHEMATIC

divides the lines along each axis into blocks (the number of lines within a block must be a power of two) which are selected one at a time. Input then proceeds in parallel to that block. The degree of parallelism involved is determined by the size of the blocks. For example, a 512×512 matrix may conveniently be divided into blocks of 2, 4, 8, 16, 32, 64, 128, or 256 lines. It can be shown that the most economical approach is to choose a partition in which the number of different blocks per axis most closely equals the number of lines per block. In the example above, this means that either 16 blocks of 32 lines or 32 blocks of 16 lines will be the most economical approach. The latter choice is actually being investigated since the 16 bit parallel input conforms to the commonly used 8×16 character matrix. Except for the cost of installing a 16 bit buffer register to provide the parallel input lines, the cost of this last technique is approximately the same as that of full serial. Figures 1-6a-c illustrate all three methods using a 16×16 matrix of discharge elements.

1.2.2 Full Screen Erasure

A valuable inherent panel capability is that of full screen erasure. Since the sustaining voltage, $V_s(t)$, functions exactly as its name implies, it is only necessary to modify $V_s(t)$ momentarily (reducing the width of a single pulse) to force the entire viewing area to the "0" state.

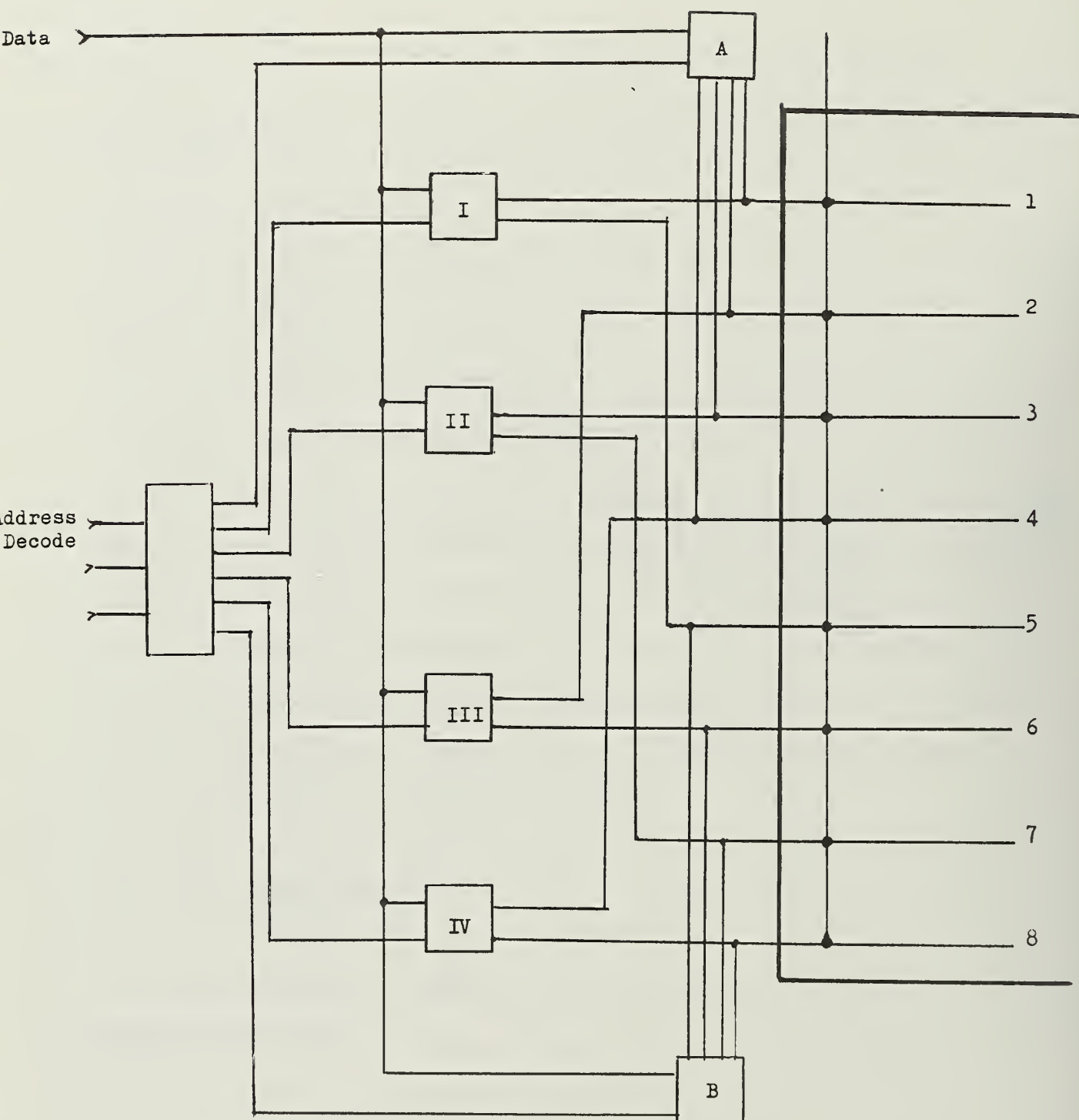


▷ = Drive Circuit

Data is input in a 16 bit parallel fashion along y-axis while one line along the x-axis is enabled.

Fig. 1-6a

PARALLEL ADDRESSING

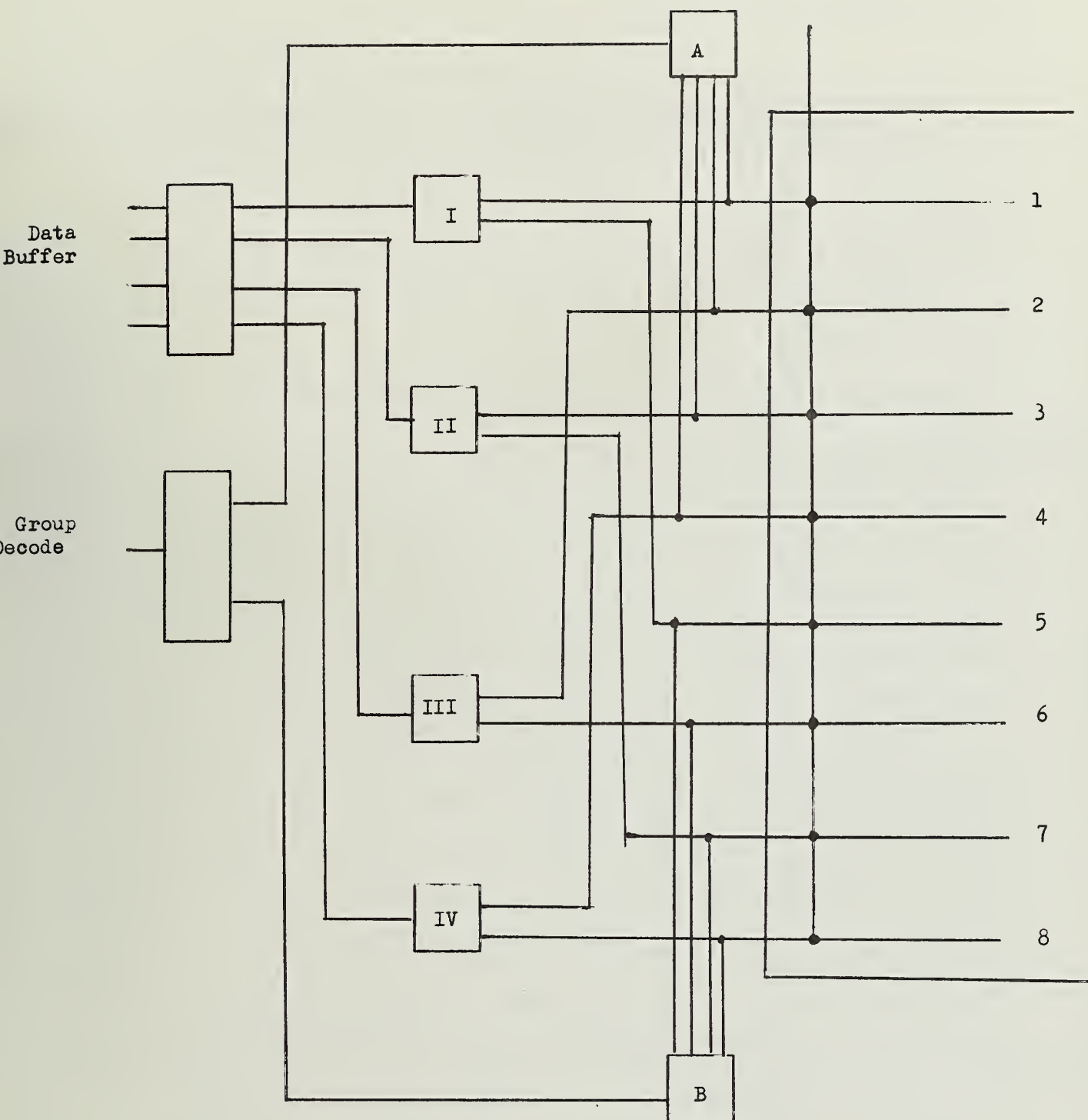


= Drive Circuit

Decoding circuit determines which line is selected to use data. Example: If A and II are enabled, line #3 is chosen. (Use same scheme on other axis.

Fig. 1-6b

MULTI-LEX (SERIAL) ADDRESSING



= Drive Circuit

The group decode circuit determines whether group A or B is chosen. Four bits of data are then input to the lines of the chosen group.

Fig. 1-6c

SEMI-PARALLEL ADDRESSING

1.2.3 Electrical Readout (10)

Another panel feature which is being investigated at the University of Illinois but which is not yet commercially available is its capacity for electrical readout of the display. This capability facilitates the implementation of several user-oriented capabilities including "rollup," text editing, hard copy, etc.. These user features will be discussed in detail in Section 3.

There are two external indications of cell state, the emitted light (See (3, 5) for a discussion of optical readout techniques) and the external current pulses resulting from the internal discharge currents which characterize the "1" state. The problem arises in detecting the current corresponding to a discharge amid large capacitive charging current and noise (Note that the panel may be represented by the lumped parameter model in Fig. 1-7). Fortunately, in the DIGIVUE[®]* line of panels (Sect. 1.4) the discharge current is delayed 200-500 ns following the initial capacitive spike. This simplifies the sensing problem considerably, eliminating the need for complex subtracting circuits. The most promising technique involves the concept of impedance insertion (Fig. 1-8). During the discharge interval $V_{sw}(t)$ goes high, placing the input impedance of the sense amplifier in series with the panel electrodes. This forces the discharge current to flow through the effective capacitance, C_e . The voltage appearing at the input terminals of the sensing amplifier is the integral of the discharge current. In practice, this is on the order of one volt.

To implement such a scheme on a real panel, the choice again must be made between cost and flexibility. Figures 1-9a and 1-9b show the

* Trademark of Owens-Illinois

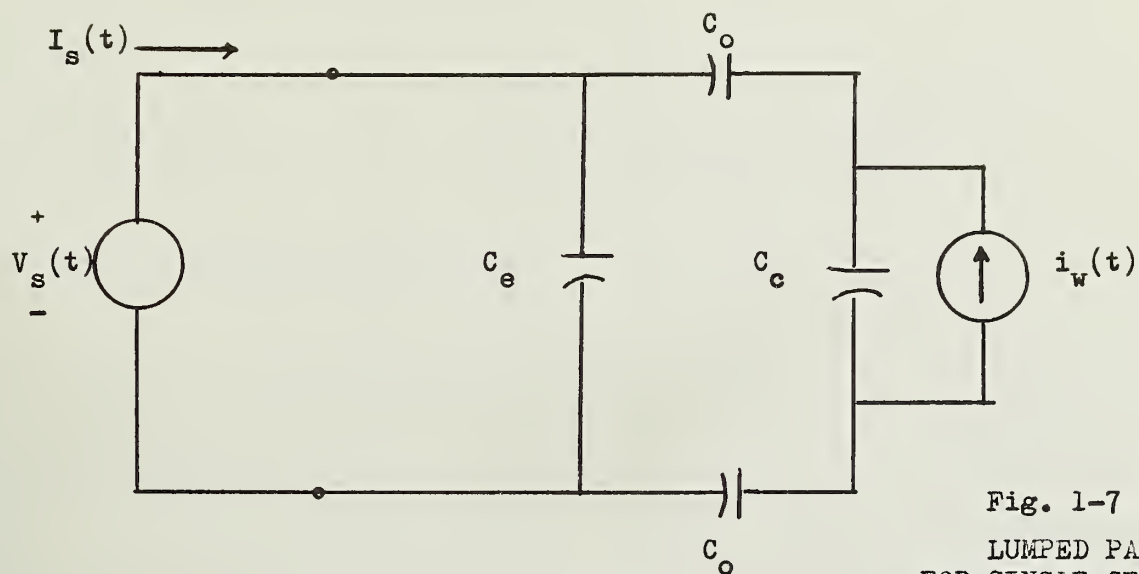
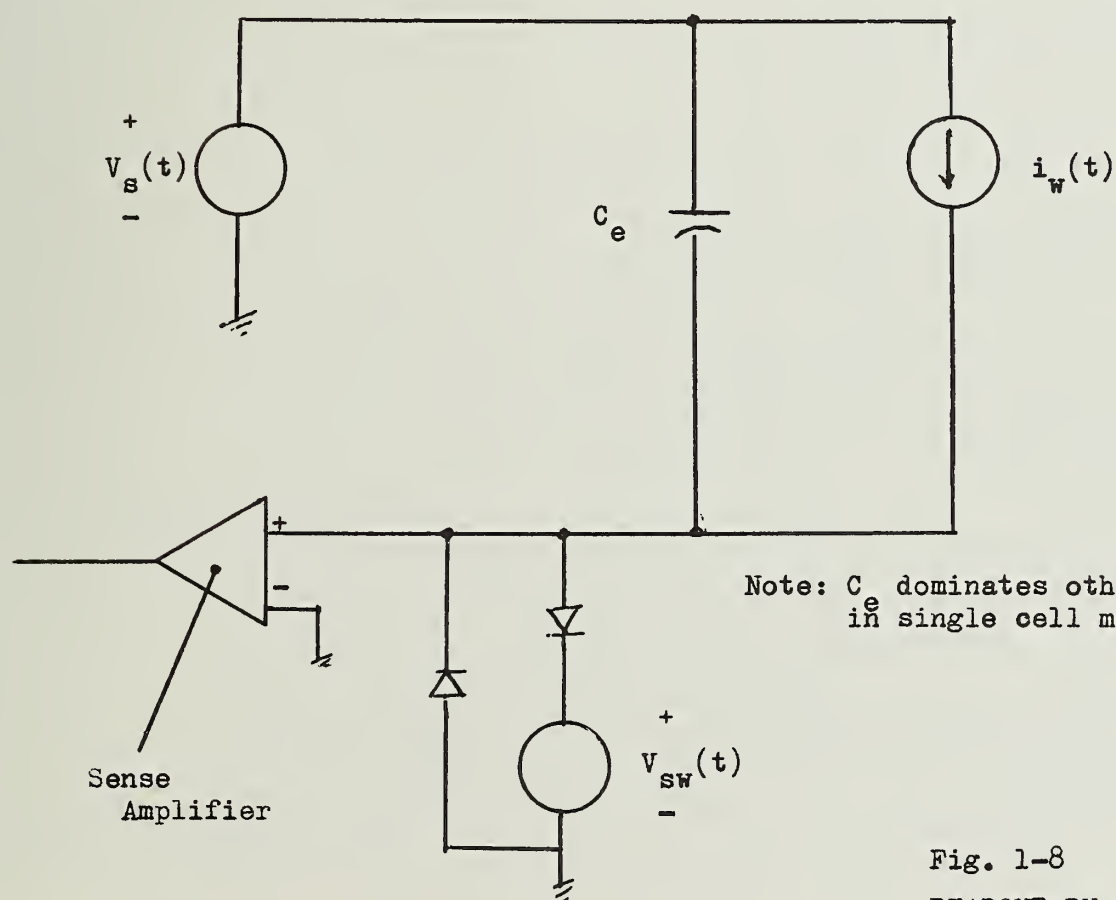


Fig. 1-7
LUMPED PARAMETER
FOR SINGLE CELL IN AN
 $N \times N$ MATRIX



Note: C_e dominates other capacitances
in single cell model

Fig. 1-8
READOUT BY IMPEDENCE
INSERTION

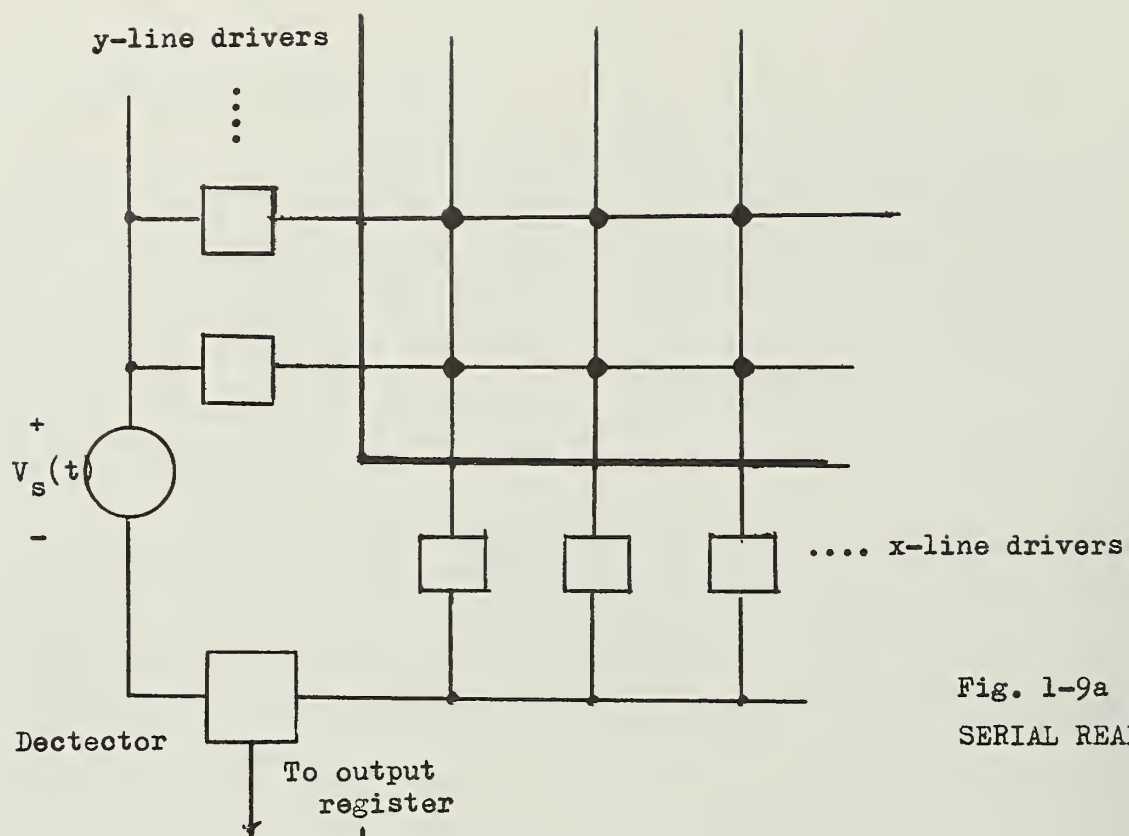


Fig. 1-9a
SERIAL READOUT

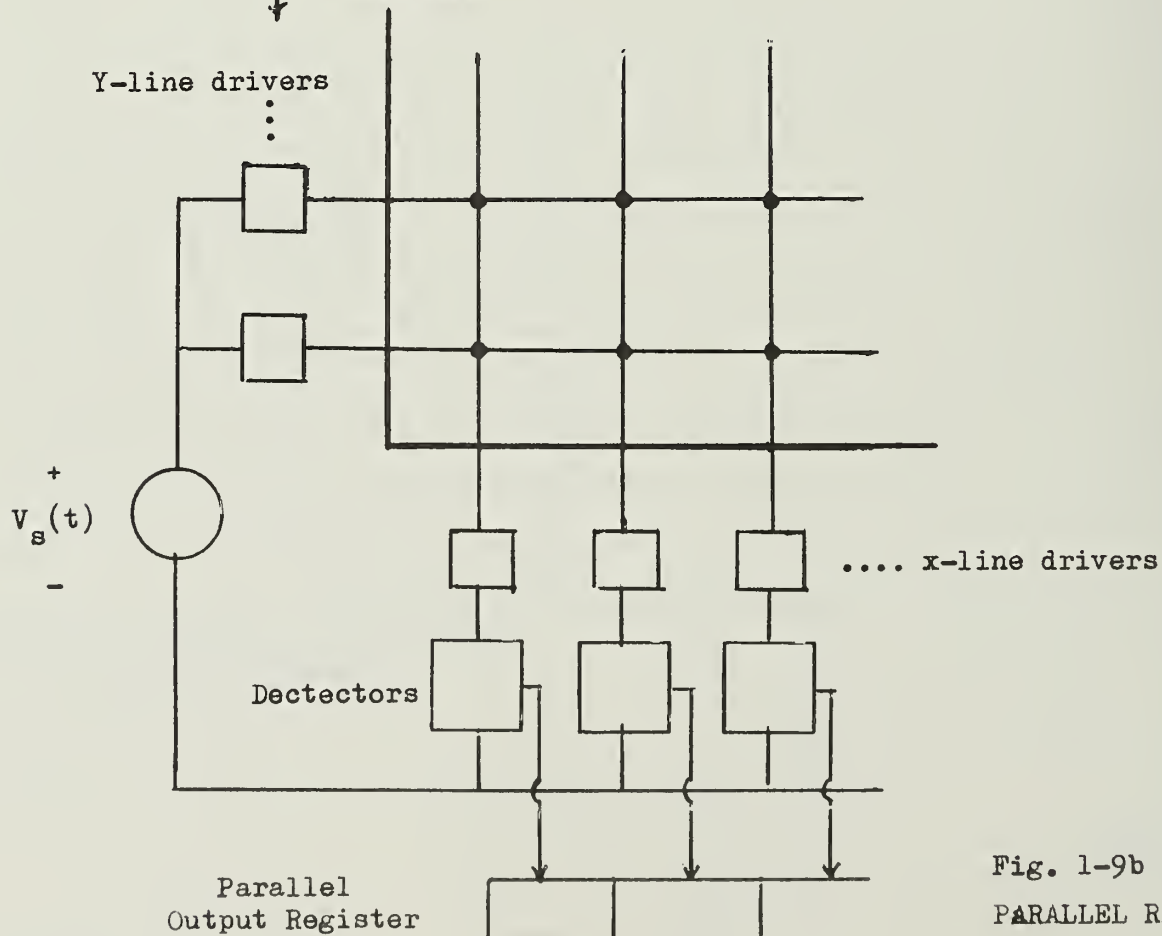


Fig. 1-9b
PARALLEL READOUT

two extreme readout configurations. A more practical scheme would involve the use of several switchable detectors feeding a parallel output register.

1.3 Display Effectiveness Factors

There are a number of characteristics which may be used to determine the usefulness of a particular display technology. This section will define these factors and use them to describe a representative commercially available panel, the DIGIVUE 512-60 (Sect. 1.4).

1. Brightness/Contrast—This parameter concerns the brightness of the light emitting element and its visibility in relation to its background.
2. Half-Tone Capability—This is the ability to generate varying levels of intensity. In many applications ON/OFF may be sufficient.
3. Color Generation Capability
4. Resolution--Involves criterion for both minimum and maximum distance between light emitting elements. Note: human visual acuity = 1 min. of arc.
5. Viewing Angle—The number of degrees of effective viewing.
6. Flicker—To be effective, a display must be regenerated more than 16-30 times per second, or it must have built-in persistence.
7. Distortion and Accuracy—These factors involve plotting accuracy. They are a function of the alignment of the display elements and their interaction.
8. Blemishes—Areas of the display which may not be activated.
9. Volume/Area—This is the ratio of the total volume of the display to its effective display area. (May also involve weight/area).

10. Power Consumption—A number of parameters may be useful here: total power consumption, power/radiated power, power/visible radiation, etc.

Display Effectiveness Factors
DIGIVUE 512-60

Parameter	Data*	Comments*
Brightness/ Contrast	50-100 fL	Due to the transparency of the display, any desired background may be inserted.
Half-Tone	-	Current commercially available panels are bistable, but work is being done to develop multi-intensity models.
Color	-	As above
Resolution	60 lines/inch d = 7 m in. Resolve = 2-3 ft.	Panels are currently being marketed with densities of 33, 50, and 60. 100 lines/inch has been achieved.
Viewing Angle	Near 180°	
Flicker	None	One of the advantages of the plasma panel is this inherent memory property.
Distortion/ Accuracy	Good	Cell interaction is virtually non-existent, and electrode layout tolerances are well beyond one's capability to notice distortion.
Blemishes	None	
Vol./Area	Small	Panel itself is only $\frac{1}{2}$ " deep and electronics may be mounted apart if necessary.
Lifetime**	5000 hrs.	Probably more. Data is not yet available.
Power Consumption	V _s = 110 v Peak Surge = 5 A. Ave. Power 200 W	Under normal use a panel will actually draw no more than 60-90 W. This works out to an average of 0.2 mw/bit.

* Numbers typical of present panels

** Estimated

1.4 Research and Commercial Availability

Further refinements of the theory described in previous sections demonstrate the feasibility of more than two stable states with varying levels of light intensity (7). Different colors are also possible. In fact, three-color panels with multiple intensity levels are now under development at Owens-Illinois (8).

It is also possible to take advantage of the transparency of the panel by superimposing rear-projected data from microfilm, slides, etc. on the dynamic, computer-generated display. Interactive communication by touch (a light pen-like capability) is also achievable. Terminals with both of these options will be used in the PLATO IV computer-based education system at the University of Illinois.

Although a number of government organizations and commercial firms (notably RADC, CDC, Fujitsu, and Owens Illinois) have been actively pursuing research in the field of plasma display technology since 1965, its commercial availability is still quite limited. Only Owens-Illinois currently offers a very limited line of displays.

Owens-Illinois Available Models

1. DIGIVUE 64-33 Display/Memory Unit—The DIGIVUE 64-33 is 64x256 lines at 33.3 lines per inch. The panel is approximately 2.1 inches by 8 inches in size and displays up to 252 characters in 6 rows of 42. Characters can be displayed in a 5x7 dot matrix or in the random-accessed graphic form across the viewing surface of over 16,000 display elements.

2. DIGIVUE 256-50 Display/Memory Unit—The DIGIVUE 256-50 is 256x512 lines at 50 lines per inch providing a $5\frac{1}{2}$ " by $10\frac{1}{4}$ " active display area for up to 2,000 characters.
3. DIGIVUE 512-60 Display/Memory Unit—The DIGIVUE 512-60 is 512x512 lines at 60 lines per inch with an active display area of $8\frac{1}{2}$ " by $8\frac{1}{2}$ " for up to 4,000 characters.

Owens basic product is the DIGIVUE Display/Memory Unit, which includes the DIGIVUE Display/Memory panel, the circuitry for driving and addressing the panel, and the necessary power supply. The unit can be interfaced at low-voltage logic levels to standard digital circuitry.

2.0 Model Development Introduction

Since the initial development of plasma display technology, many systems have been envisioned which incorporate this new device. These range from associative memory systems to actual display terminals. To actually build such systems though, it is necessary to know just what performance specifications are achievable and what capabilities can be provided. A mathematical model provides the tool by which such "paper" systems may be described and tested without actually being built. A model of the plasma display/memory unit will therefore be introduced at this point to facilitate future discussion of possible display terminal designs.

For the purposes of this model, the plasma display/memory unit will be defined to include the panel itself, the electronics necessary to receive TTL or similar digital inputs (of appropriate format—Sect. 2.1.2) and generate a display, and the required power supplies. Also included will be the digital communication lines to the unit and its visual output. See Figure 2-1 for a block diagram of the model. Note that this definition does not encompass the entire display terminal. Related hardware such as line and character generators, local memory, and a user keyset are not included.

As shown in Fig. 2-1, the model may be divided into three sub-sections, communication, the panel itself, and its visual output. The remainder of this section will be involved in a more detailed discussion of these components.

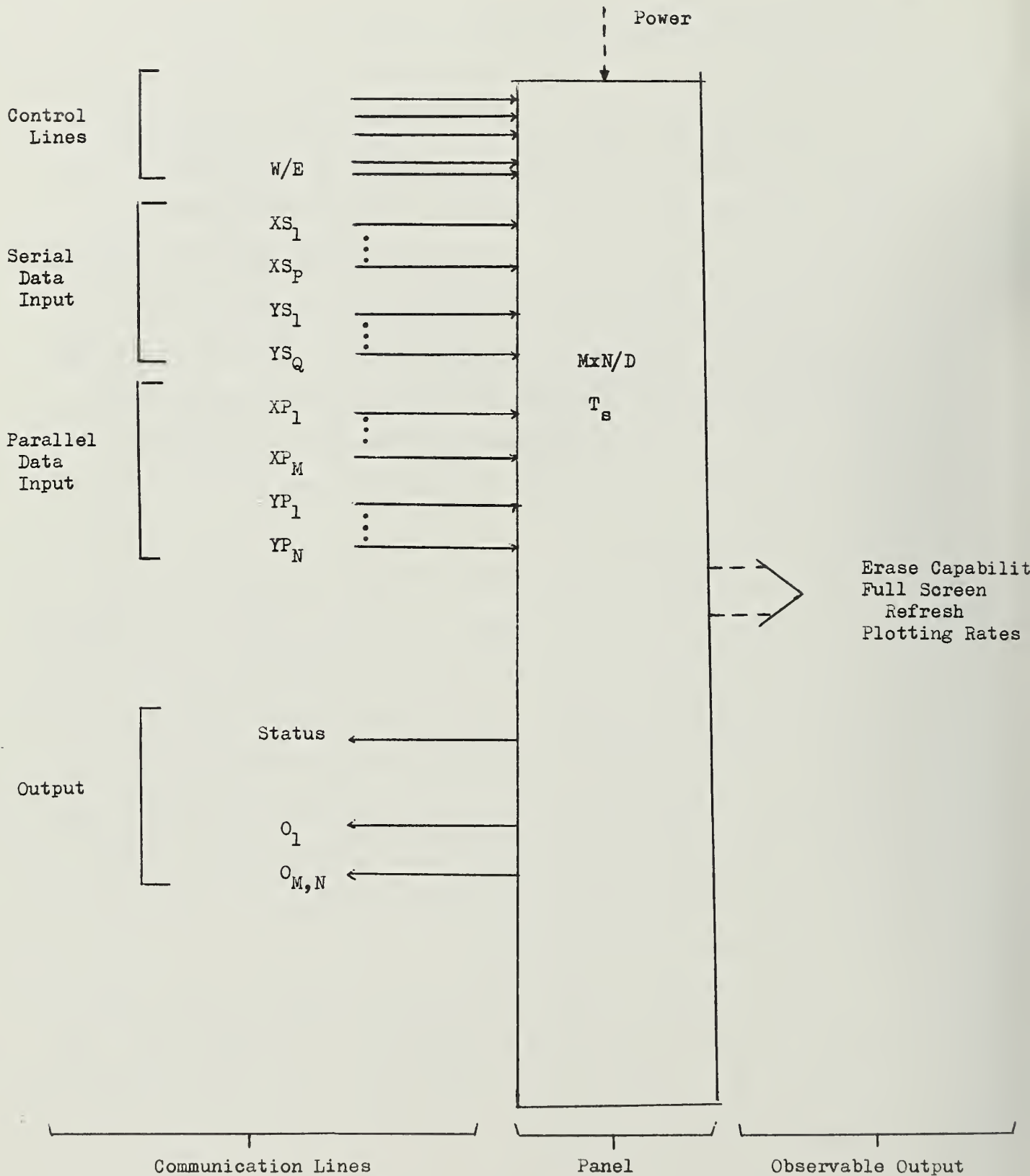


Fig. 2-1

PLASMA DISPLAY/MEMORY UNIT MODEL—
BLOCK DIAGRAM

2.1 Model Description

2.1.1 Panel

The subsection labeled PANEL in Figure 2-1 is actually used to represent gross unit characteristics, primarily display surface parameters and power requirements.

I. $M \times N/D$ —These letters refer indirectly to the size and resolution of the display area. " $M \times N$ " indicates the number of display elements along the x and y axes respectively. "D" gives the density of the elements along both axes in units of number per inch.

T_s —This is the period of the sustaining voltage, however it is more useful to think of it in terms of a time per operation. For example, in full serial operation, one point may be addressed every T_s seconds.

II. Power—A typical plasma display/memory unit requires several different power supplies. These include the sustaining voltage (V_s), the x-y select voltages (V_p), the logic voltage (V_L), and the interrogate voltage (V_I). Maximum and average currents must be specified for each supply. The total average power drain may then be used to compute a power/display bit figure.

2.1.2 Communication Lines

Digital communication with the unit consists of TTL compatible input and output lines. The input set may be further broken down into three subsets, control, serial data, and parallel data lines.

2.1.2.1 Control Lines

There are five basic control options:

1. E_S —full screen erase
2. E_B —block erase. A rectangular array of display elements are erased in one operation.
3. W/E^* —write or erase
4. P/S —parallel or serial. This bit indicates the type of data transfer involved.
5. I —interrogate. This bit initiates electrical readout of the display.

From these options seven distinct operations may be defined:

1. Write—Parallel
2. Write—Serial
3. Erase—Parallel
4. Erase—Serial
5. Full Screen Erase
6. Block Erase
7. Interrogate

* Although the W/E option may be thought of as a bit in the control word, this line is usually used as a 2-wire input, apart from the control bits, to initiate a timing sequence for the operation indicated by the rest of the control word.

Of these, note that five are determined by the "real" control bits. Thus in the most general case, three bits are needed to deliver these functions. Of course some terminals may not have all of these features and might therefore require fewer bits.

Possible Control Word Configuration

000	Full Screen
001	Block Erase
010	Parallel Input
011	Serial Input
100	Interrogate

2.1.2.2 Serial Data Input

In this mode of operation data is received and displayed one point at a time. If the panel has $M \times N$ addressable points (where $M = 2^P$ and $N = 2^Q$), the unit may have up to P "x" lines, designated XS_i : $i = 1, \dots, P$, and Q "y" lines, designated YS_j : $j = 1, \dots, Q$. When the unit is receiving data in the serial mode (control code = 011), the binary value of $\{XS_i\}$ and $\{YS_j\}$ are interpreted as the x,y address of the point to be referenced. On the other hand, if the unit is operating in a parallel mode (control code = 010), the address along each axis is interpreted as the starting address for a block of data to input in parallel (See next section).

Example: Given the following input configuration:

$XS_i = 11111111$; $YS_j = 000000011$

Control Code = 011

Write Timing Sequence

The 3rd element in the 512th row of the matrix will be turned on.

2.1.2.3 Parallel Data Input

In this mode of operation each axis of the screen is divided into B blocks (the number of lines contained in a block must be a power of two). If R = the number of lines contained in each block, and $R = 2^T$, then $B_x = 2^{P-T}$ and $B_y = 2^{Q-T}$. Since the number of x, y parallel lines, designated XP_k and YP_l ($k = 1, \dots, R_x$ and $l = 1, \dots, R_y$) may range up to M and N respectively, $R_x = M$ and $R_y = N$ in the most general case.

Each parallel operation consists of placing a block of data on either the XP or YP lines. That block's base address is simultaneously placed on the serial lines XS or YS , and R_x or R_y bits are read in in one operation.

Example: Given the following input configuration:

$XS_i = 000000000$; $YS = 000000001$

$XP_k = 111111111$;

Control Code = 010

Write Timing Sequence

Sixteen one bits will be written in rows 0-15
of the 2^{nd} column.

2.1.2.4 Output Lines

Output consists of either the result of electrical readout or the panels' status. Since panels are commonly operated asynchronously, the latter is used to indicate a terminal busy condition. The former consists of direct data readout from the display. The degree of parallelism is determined largely by cost factors, but in general may

be up to the number of lines along either the x or y axis. Thus, if the output lines are designated $\hat{O}_h$: $h = 1, \dots, \max(M, N)$. When a block of data is being read out, the base address of the block appears on the serial data lines and the data is read out in parallel.

Example: Given the following input configuration: (8 bit output)

$XS_i = 000000000$; $YS_j = 000000000$

Control Code = 100

The first eight bits of the first row are read out and appear in the parallel output register.

2.1.3 Visual Output

The observable output of any display terminal may be characterized by a few basic parameters. These will include:

1. Erase capabilities and rates
 - a. Full screen
 - b. Block
 - c. Other
2. Full screen refresh rate
3. Plotting rates
 - a. Point
 - b. Character (n x m character matrix)
 - c. Line

2.2 Four Illustrative Models

This section will introduce a family of plasma displays described by the modeling process presented in Section 2.1. Following each model, the display's output characteristics will be reviewed. To facilitate the discussion, gross panel characteristics will be assumed constant. All panels will be constructed such that $M = N = 512$, $D = 60$, and $T_s = 20$ mms.

2.2.1 Full Serial Model

Model I (Fig. 2-2a) is the only model of the four to be discussed which is now commercially available. It corresponds directly to the DIGIVUE 512-60. This display requires a 19 bit parallel input (Fig. 2-2b) and a single output line (status) operating at a maximum rate of 50 KHz. Data is plotted point by point. Since a basic operation time of 20 mms has been assumed, a single character (plotted on an 8x16 dot matrix) can be displayed in $128 \cdot 20$ mms = 2.56 ms.

Plotting Rates

Point	50,000 points/sec.
Character(8x16)	390 chars./sec.
Line	833 inches/sec.
Full Screen Refresh	5 sec.

When erasing data, this unit is somewhat more flexible. Specific points still must be turned off at the same 50 KHz rate, but the entire

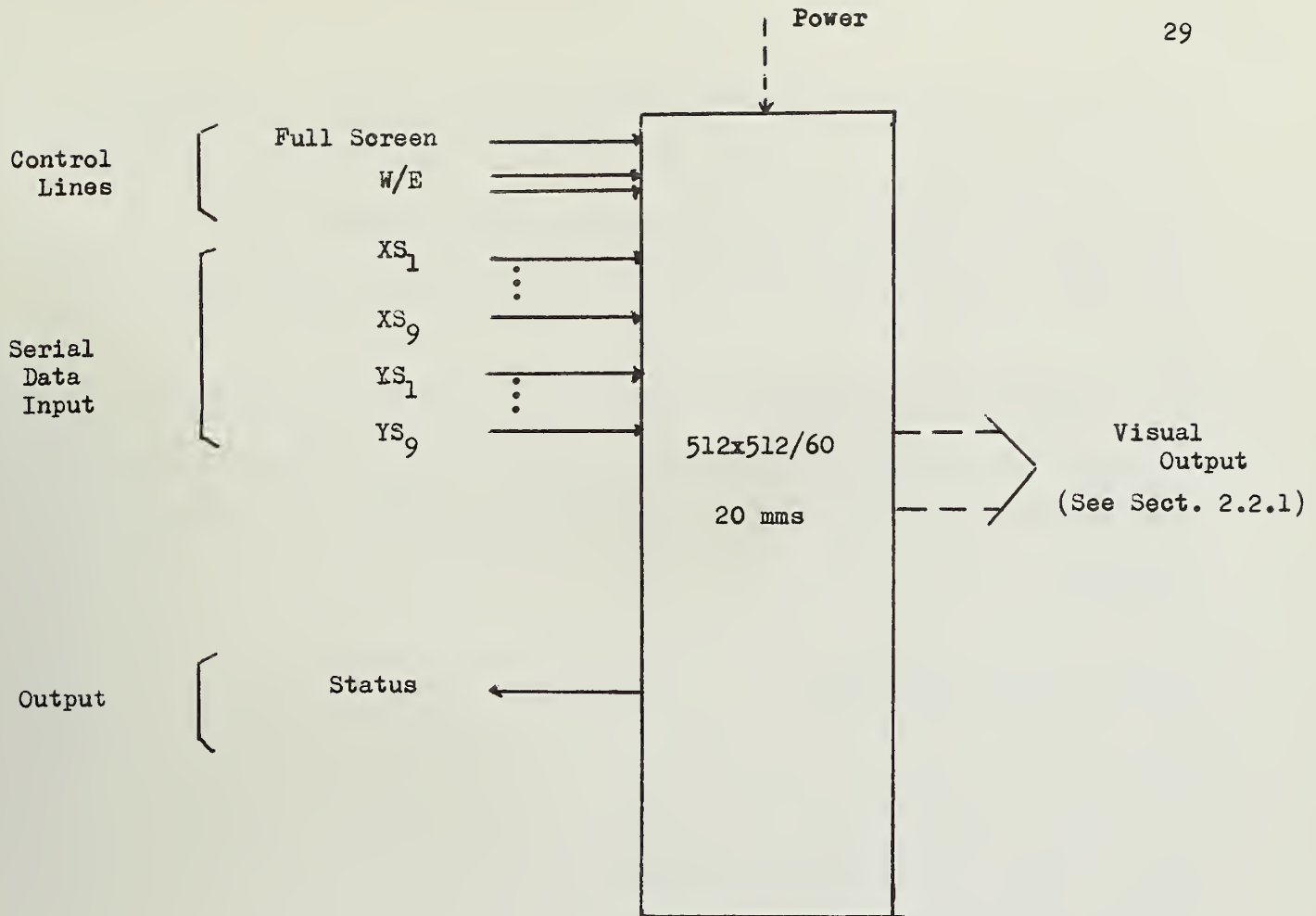


Fig. 2-2a

MODEL I

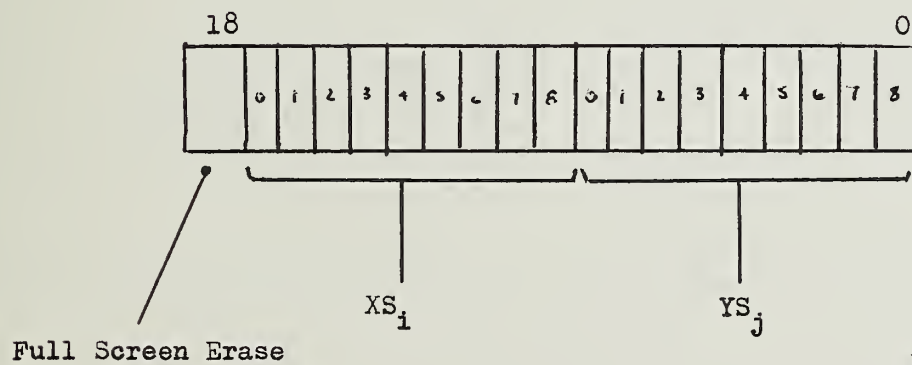


Fig. 2-2b

INPUT DATA WORD
(MODEL I)

screen may be turned off in one operation (Sect. 1.2.2). In addition, if an extra address bit is added, it is possible to turn on or off an entire row or column of elements. Erasing a row of 8x16 element characters then requires $1/512^{\text{th}}$ the time required in a totally serial mode.

Finally note that Model I has no electrical readout capability. This negates the possibility of hard copy and also has ramifications in situations requiring display shifts. This problem will be discussed in Section III.

2.2.2 Full Parallel Model

Model II (Fig. 2-3a) is identical to I in all respects except that I's serial input has been replaced by full parallel along the y-axis. This display therefore requires a 612 bit parallel input (Fig. 2-3b). Data is displayed along one axis 512 points per operation.

Plotting Rates

Point	2.56×10^6 points/sec.
Character(8x16)	200,000 chars./sec.
Lines	Full vertical in 20 mms, All other at 833 inches/sec.
Full Screen Refresh	.01 sec.

This display is extremely fast when displaying columns, but relatively slower when the display points are more randomly distributed. An extremely attractive feature of this full parallel model is its ability to erase (or turn on) blocks of varying sizes and location.

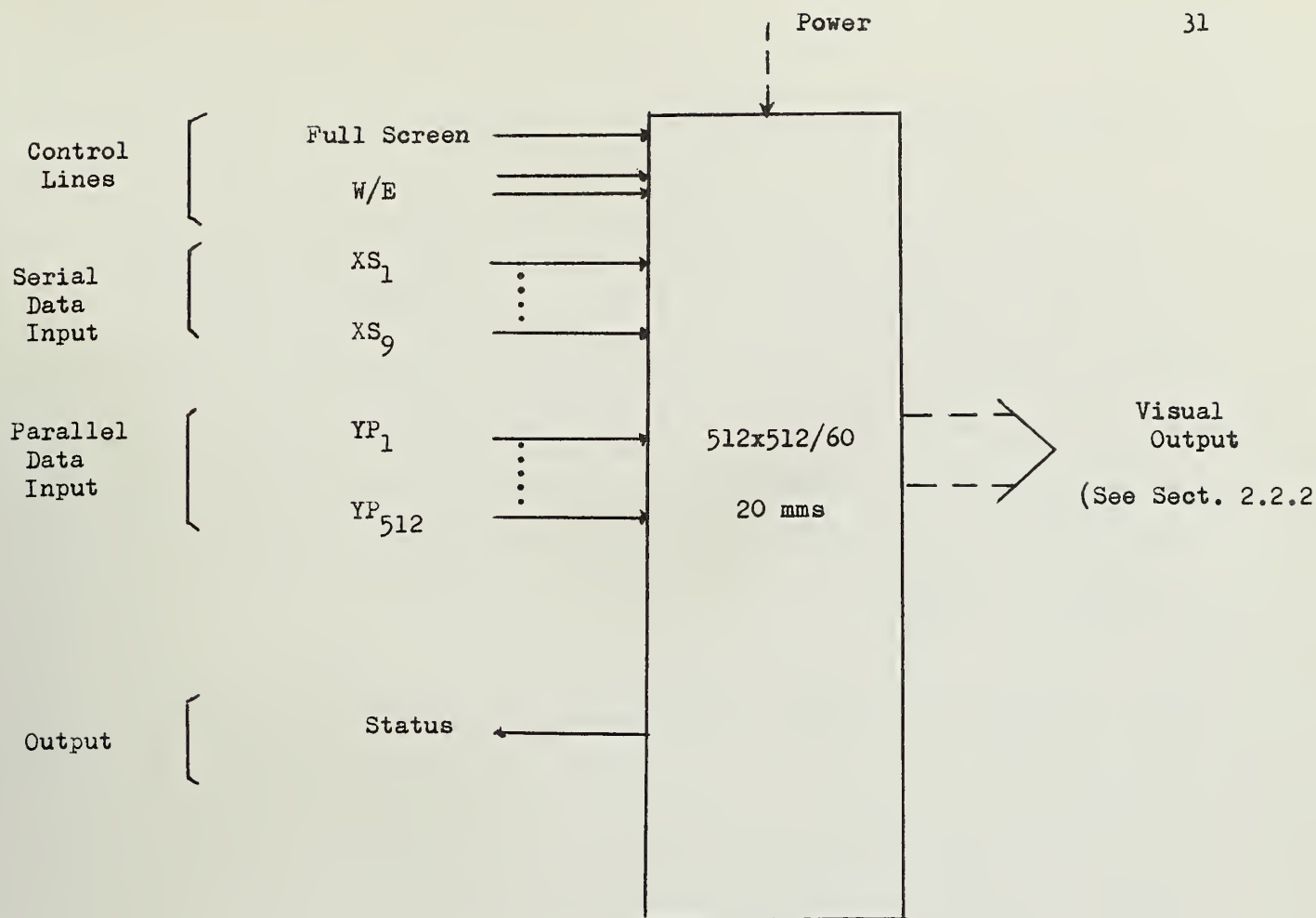


Fig. 2-3a
MODEL II

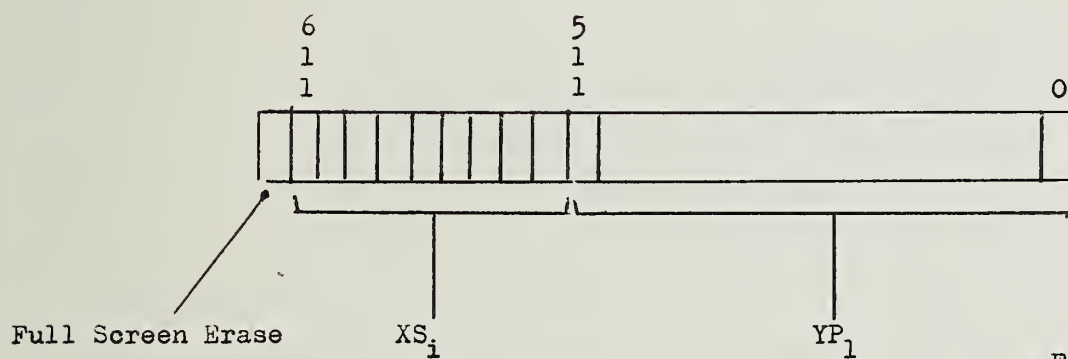


Fig. 2-3b
INPUT DATA WORD
(MODEL II)

2.2.3 Full Serial Model With Electrical Readout

Model III (Fig. 2-4a) is identical to I except an 8 bit parallel electrical readout capability is added. In this case then, the display requires a 20 bit parallel input and a 9 bit parallel output (Fig. 2-4b), both operating at a maximum rate of 50KHz. Note that the 8 bit output is chosen to match the x-axis of the standard 8x16 character matrix. A single character may therefore be readout in 8 cycles or 160 nms.

2.2.4 Semi-Parallel Model With Electrical Readout

Model IV (Fig. 2-5a) has a 16 bit parallel input as described in Section 1.2.1 in addition to III's readout capability. It requires a 53 bit parallel input (Fig. 2-5b) and a 9 bit output. Its plotting rates are based on its capability for plotting 16 points per operation.

Plotting Rates

Point	800,000 points/sec.
Character(8x16)	6,250 chars./sec.
Lines	13,000 inches/sec.
Full Screen Refresh	.33 sec.

This display scheme has a number of advantages. It is now possible to block erase a 16x16 point area. Since this corresponds to two characters, text erasures are easily implemented. Note also that its writing capability--16 points per operation--is also based on

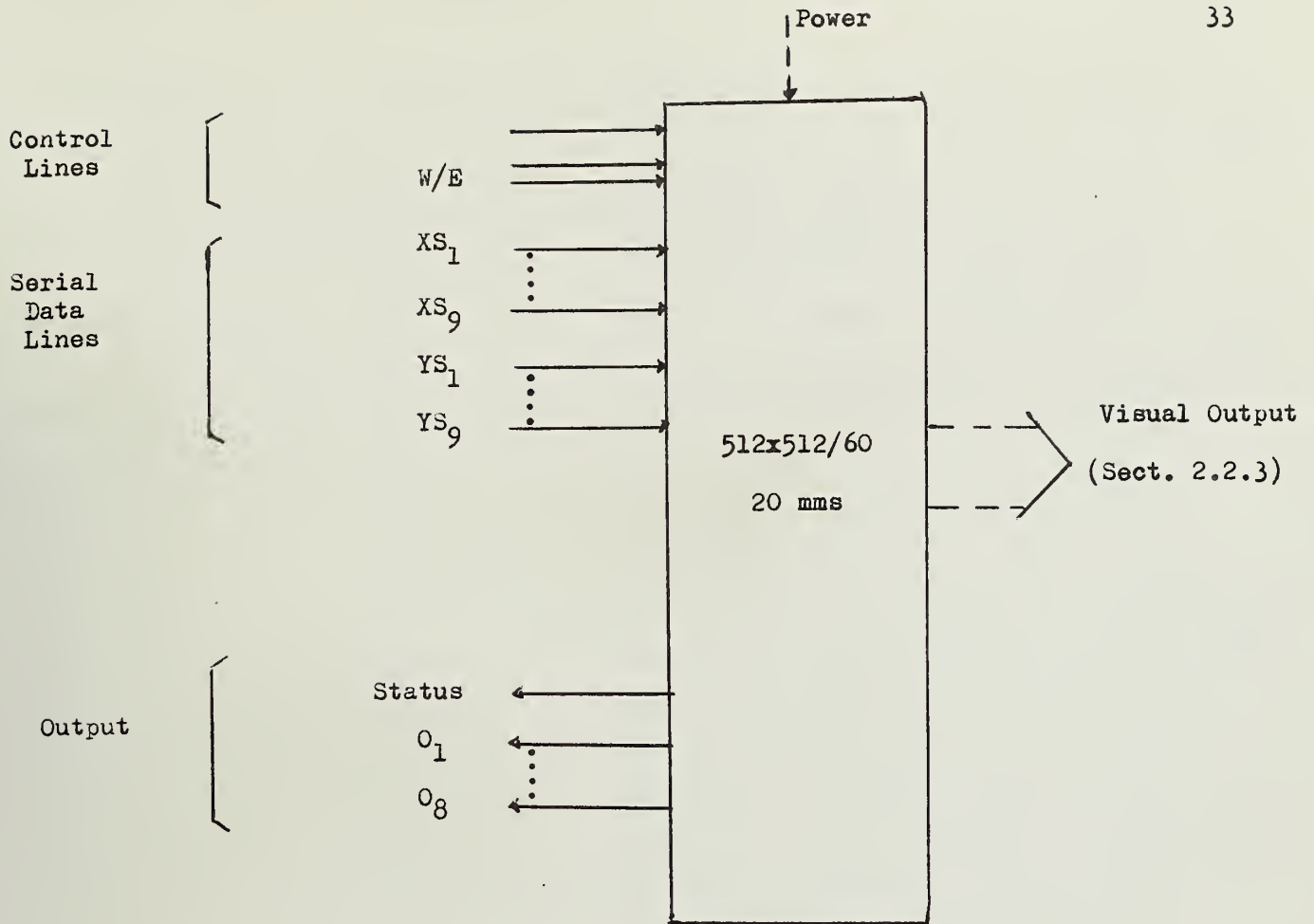


Fig. 2-4a
MODEL III

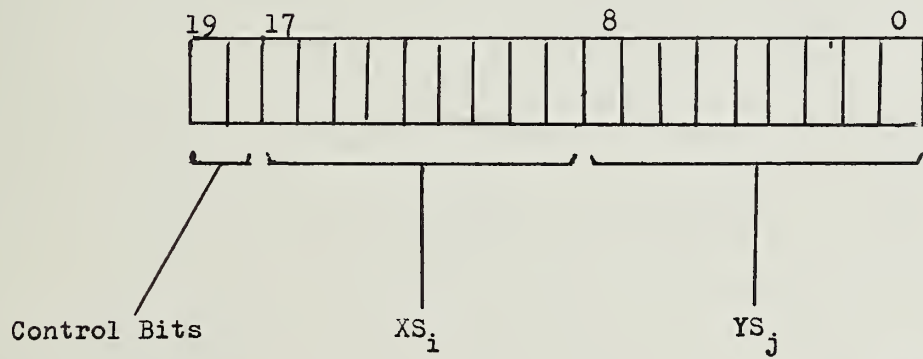


Fig. 2-4b
INPUT DATA WORD
(MODEL III)

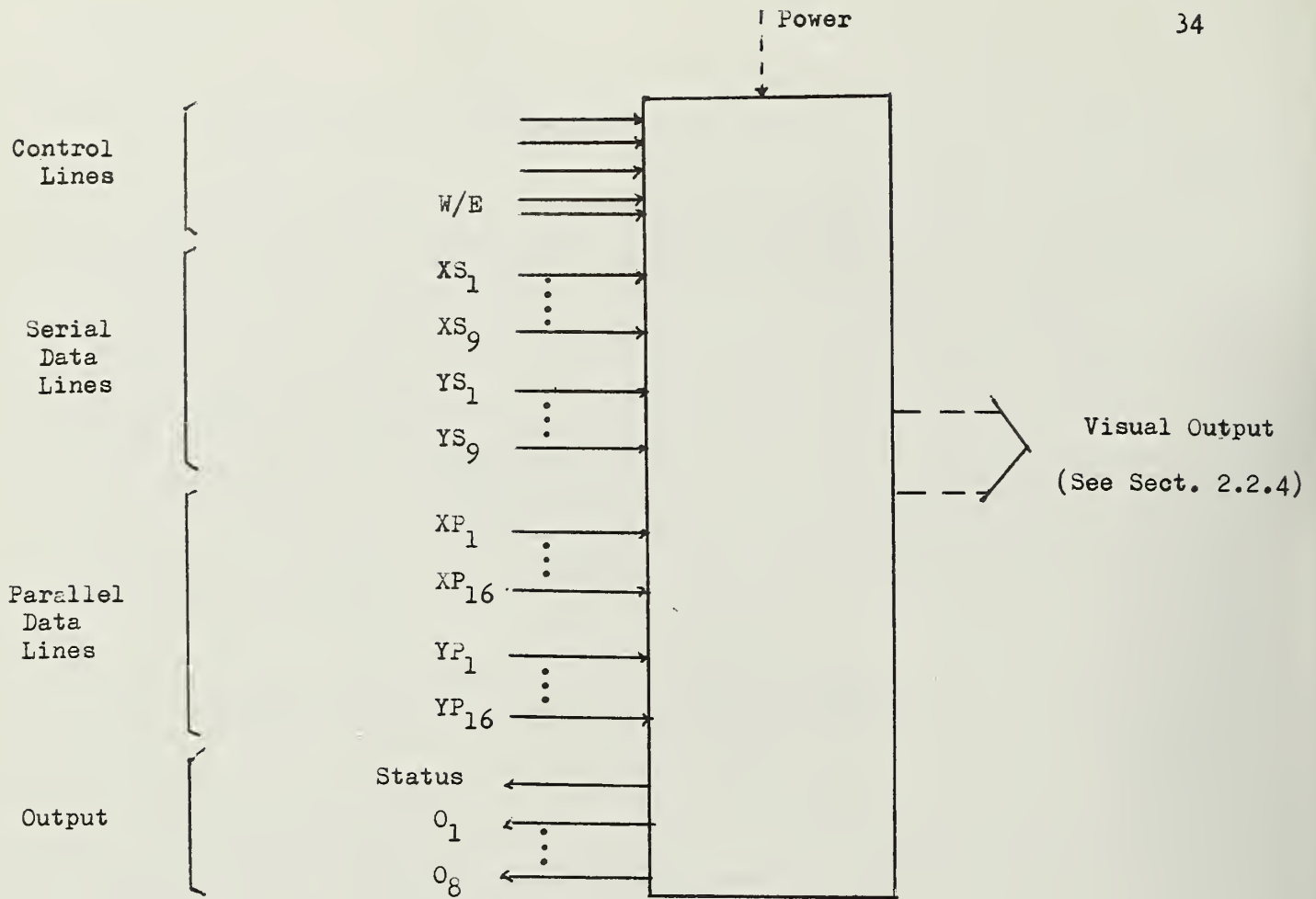


Fig. 2-5a
MODEL IV

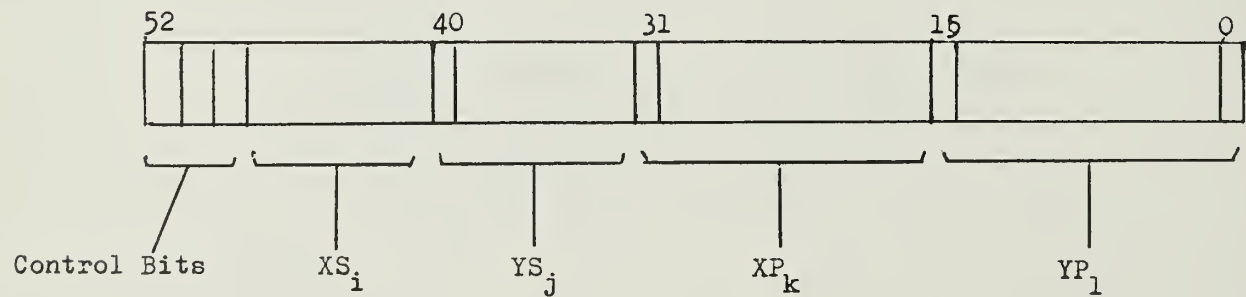


Fig. 2-5b
INPUT DATA WORD
(MODEL IV)

character size. Large block erasures might be implemented using a series of 16x16 erasures. One drawback of this technique though, is that, unlike full parallel block erasure, in this model the block base addresses are fixed, so some flexibility is lost in formatting the display area. For instance, radically different portions of a display (eg. graphs and text) should not overlap 16x16 boundaries or they can not be treated independently.

3.0 Overview

This last section will expand its view beyond the basic display/memory unit to the whole display terminal. The PLATO IV terminal (9) will be described as a basis for discussion and then will be modified to incorporate the various display unit models discussed in Section II. Secondly, the whole spectrum of terminals incorporating plasma panels will be viewed from the standpoint of user-oriented features, and finally, drawing on all preceding sections (esp. 3.2), the advantages and drawbacks of using plasma display/memory units in display terminal applications will be discussed.

3.1 Terminal Design

The plasma display/memory unit is the primary component in a display terminal incorporating this technology. In addition, except for variations in the display module, there need be little difference from one terminal to another. It will therefore be useful to discuss a basic terminal design and then use it to describe terminals which incorporate different display units. The PLATO IV terminal ((9), used in the PLATO IV computer-based education system) will be used as an example of this basic design. A modified block diagram of this terminal appears in Figure 3-1.

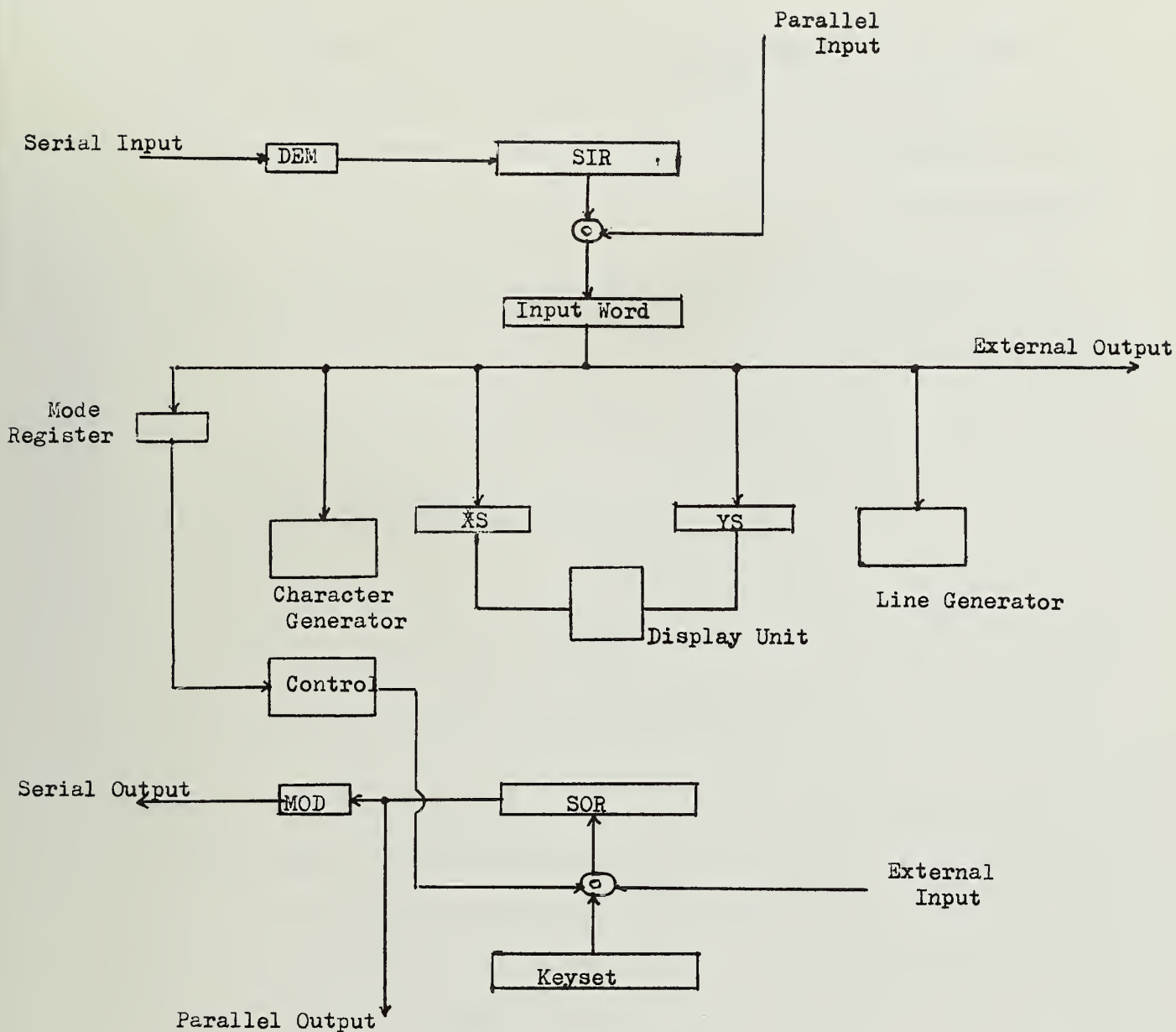


Fig. 3-1

BASIC TERMINAL (BLOCK DIAGRAM)

3.1.1 PLATO IV Terminal

The PLATO IV terminal receives data serially over a 1200 bps channel (Note provision for possible parallel input). The terminal builds up this input into 20 bit words and interprets them in four different modes:

1. Control—non-display; performs other terminal functions.
2. Point—plots points; data is input one point per word directly to the display unit.
3. Character—plots characters; data is formatted three characters per word and input to the character generator (an ROM) which then generates the character dot matrix.
4. Line—plots lines; each word in the line mode represents the end point of a line segment. These are input to the line generator which then generates the intermediate points to be plotted.

Note that this is the first mention which has been made of either line or character generators. Previously, all data was assumed to be plotted in a random-access mode. Plotting rates were only limited by the display model in question. Character and line generators become useful in situations where plotting is limited wholly by external data transmission rates. For instance in the PLATO IV terminal data points are received one per $1/60^{\text{th}}$ second. The maximum plotting rate in a normal random-access mode would only be 60 point/sec. It would take over 2 seconds to display an 8x16 character. The character generator however is actually an ROM capable of shifting

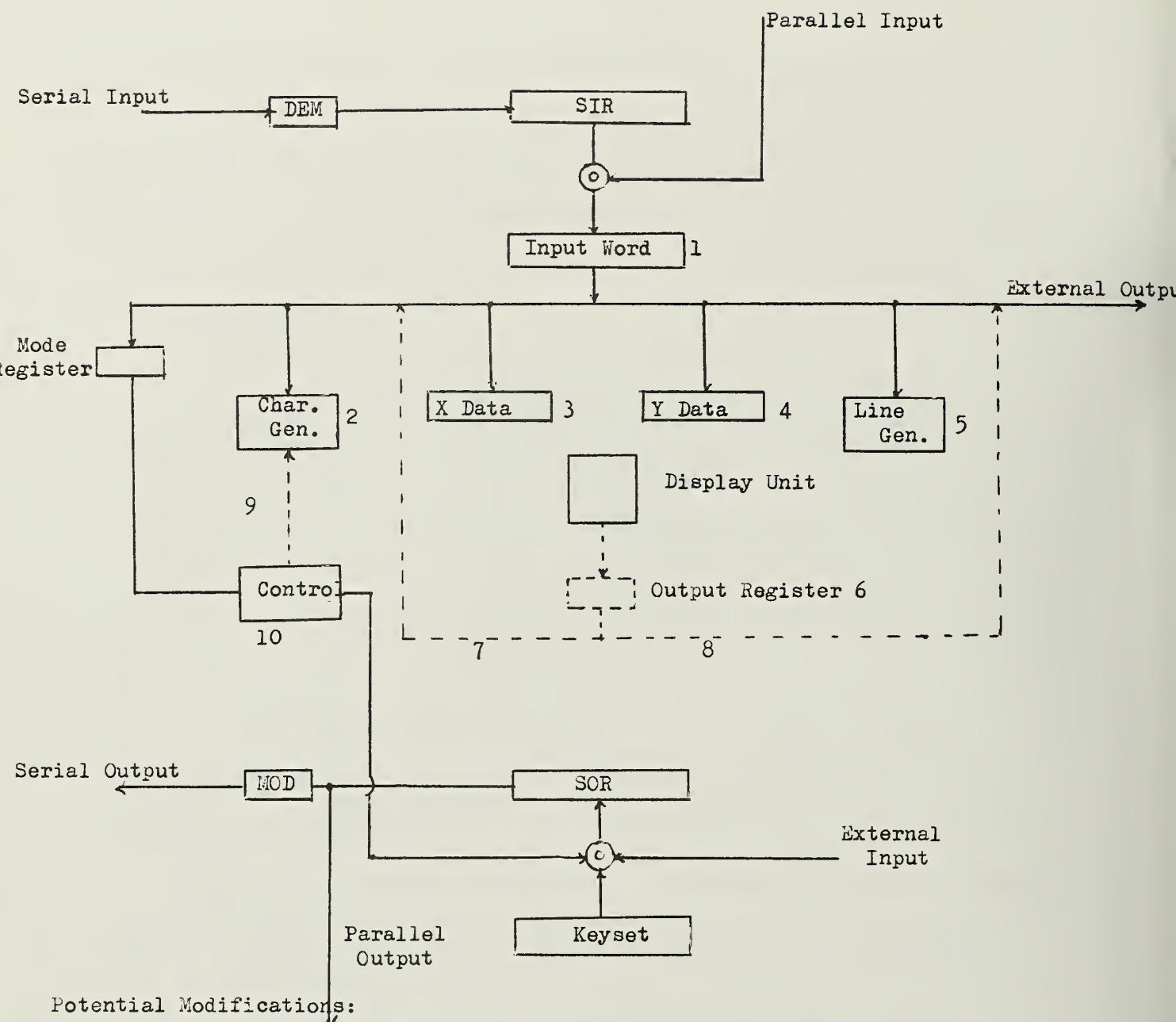
out the 128 bit matrix at rates which make the capabilities of the display unit the limiting parameter. Since the terminal receives three characters every $1/60^{\text{th}}$ second in the character mode, the terminal is capable of writing text at 180 characters/sec.

From the 20 bit input register data is routed throughout the terminal according to the word's control options. A 64 character keyset is included to give the user direct communication with the source computer. The PLATO IV terminal also has an external channel to a random-access slide projector. In general, this type of channel may be used for any sort of external equipment.

3.1.2 Modification of Basic Terminal (Fig. 3-2)

PLATO IV incorporates a display unit which is identical to that of Model I with the addition of character and line generators. Note though, that for external serial data transmission rates of greater than 1.0 MHz, no character or line generators would be necessary. In fact, some sort of buffer would be required to receive the data, since the display unit is limited to a 50 KHz plotting rate.

Model III includes electrical readout. The data input configuration of a terminal using III would be identical to that of the basic terminal, but this added readout feature would require a buffer register to receive the output data. The contents of this register could then be routed either to a peripheral data channel for hard copy output or internally for display modification (Sect. 3.2).



Potential Modifications:

- 1, 3, 4 Variable length and format dependent on model used.
- 2, 5 Modified to conform to type of input required.
- 6 Register for electrical readout (Models III, IV).
- 7 Readout used to reformat display.
- 8 Readout used to produce hard copy.
- 9 Used for internal generation of blank characters for block erase (Model IV).
- 10 Modified as required by model capabilities.

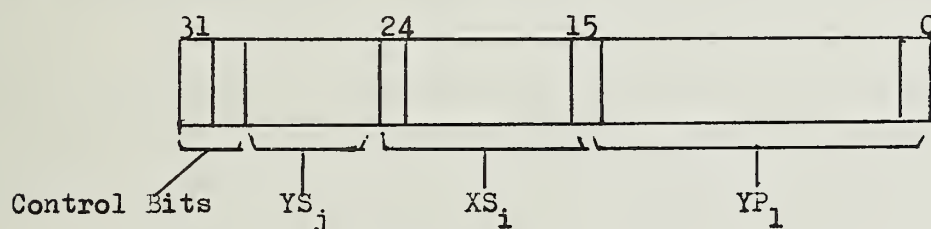
Fig. 3-2

TERMINAL MODIFICATIONS

Model IV is the only real departure from the basic PLATO IV display unit. This model may be used solely to provide a block erasure capability, to input data in a semi-parallel fashion, or both.

A terminal designed for the first application would require additional control circuitry to generate the block erasure. For instance, three successive data words (same length and format as basic terminal) could set the block erase mode and provide the beginning and ending addresses of n blocks to be erased. The terminal would then generate the data (two blank characters per block) and addresses of all intermediate blocks internally. Finally, an additional bit would have to be added to the data word to provide the block erase control capability.

For the second application, the basic terminal's input data word would have to be modified. In general, the modified word would contain 53 bits (Fig. 2-5b), but in practice this number could be reduced to 32:



Because of this increased word size, more characters could be input for each word, however, since display unit is capable of much increased plotting rates, the bottleneck is still external data transmission. Finally, note that the format of characters within the ROM character generator would have to be examined to insure compatibility with the 16 bit at a time input.

3.2 User-Oriented Capabilities

Most of the standard features of any CRT display terminal are easily implemented using plasma panels, and in fact are demonstratable on the PLATO IV terminal. These include a moveable cursor, line feed, carriage return, etc. Graphics can also be implemented although it might be worthwhile to note that its quality is somewhat limited (although much less than might be expected) by the resolution of the display elements. Several other desirable terminal characteristics deserve a little more detailed attention. These include variable format character plotting, selective display erasure, text editing, and "rollup."

1. Character plotting via a PLATO IV-type ROM character generator essentially fixes both character format and size. However, the character generator also includes an RAM in which the user may define a new character set. In addition, software-controlled plotting in a random-access point mode, provides virtually infinite flexibility in character size and type.
2. In addition to its use for speedy character or line erasure, the block erase feature described in Model IV makes possible other useful display capabilities. If it is desired to modify graphical occupying only a small part of the display area, it is not necessary to alter the remainder of the screen. It is possible to block erase the affected area and transmit new data to be displayed in its place. (Note the inherant screen formatting requirement.)
3. An identical procedure may be followed for text editing. For example, to insert a line in a body of text, it is possible to block erase the text from that line to the end and then retransmit

the affected portion of the display including the new line. PLATO IV, without this capability is, in general, forced to erase the whole screen and retransmit the entire page.

4. Page rollup is a somewhat more difficult problem with plasma displays. When the screen is filled with text, it may be desirable to "rollup" the display, eliminating the first line of text making room for the next one. There are two possible means of accomplishing this with the present technology. First, and by far the simplest method consists of transmitting an image of the modified display from the source computer. Obviously this could be extremely time-consuming--especially with a serial panel. A more complex method of accomplishing the task involves an electrical readout capability. First, a single line of text or (more efficiently) a group of lines at the top of the page would be block erased. Then each succeeding line would be read out and recopied to top of the display. Note that this method would not be limited by external data transmission rates. If Model IV were used, the time consumed by rollup would be on the order of 0.3 seconds (if readout is 16 bit parallel).

3.3 Conclusions and Recommendations

It appears that plasma displays represent a valuable advance in display terminal technology. They have the advantage of being a relatively inexpensive means to achieve a graphic capability. Plasma panels also exhibit inherent memory and consequently no flicker; they are capable of block erasure and an almost unlimited flexibility in character plotting in addition to providing most other typical CRT terminal capabilities.

Unfortunately, there are drawbacks. Current panels exhibit relatively slow replotting times for applications such as text editing and "rollup." The latter problem, though, might be circumvented. Often it is not necessary to display a whole page of text. For example, files may be examined 4 lines at a time (as opposed to a whole page). The maximum replotting time required would then be reduced to about 0.5 seconds even in a full serial display. One final problem is the inability of current displays to provide hard copy. This capability is being developed at Owens-Illinois and may become available in the relatively near future.

As stated initially, CAC has two potential uses for a plasma display terminal--on the ARPA net and with a local machine. In the former case, the terminal will be limited by serial data transmission rates of 110-2400 bps. It would be possible to use a PLATO IV-type terminal in this application (note that the increased rate of character reception at the high transmission rate would tax the display unit close to its maximum rate of 390 characters/sec.). As noted previously, if the software were designed to reduce the need

for capabilities such as full-page rollup, this currently available terminal would perform quite capably (although less well at the lower end of the transmission rate range). It could work even better in the second case since parallel input channels might be used.

In conclusion, the set of plasma display/memory units which are presently available would probably be quite capable of satisfying most of CAC's needs at a relatively low cost (it is estimated that the terminal described in (7) can be produced in quantity for less than \$2500—a fraction of the cost of a comparable CRT graphics terminal.)

However, the technology does exist to provide vastly improved display units—incorporating electrical readout (for hard copy and editing), a 16 bit semi-parallel data input (for block erasure and rapid plotting). Consequently, Owens-Illinois should be consulted regarding a terminal incorporating these features.

References

1. Control Data Corporation, "Large Screen Plasma Display," RADC-TR-71-133, July, 1971.
2. H. G. Slottow, "The Plasma Display Panel--Principles and Prospects," Owens-Illinois Electro/Optical Display Development Technical Bulletin #DU-100, May 21, 1971.
3. R. L. Johnson, "The Application of the Plasma Display Technique to Computer Memory Systems," Coordinated Science Lab, University of Illinois, Urbana, Ill., Rep. R-461, April, 1970.
4. H. G. Slottow and W. D. Petty, "Stability of Discharge Series in the Plasma Display Panel," IEEE Trans. on Electron Devices, Vol. ED-18, #9, September, 1971, pp. 650-654.
5. Bitzer, et. al. "Gaseous Display and Memory Apparatus," patent Ser. No. 3,559,190 Jan. 26, 1971.
6. Zinn and Schlam, "Guidelines for Solid-State Flat Panel Displays, Part I, Display Effectiveness Factors," R and D Technical Report, ECOM-3384, Jan., 1971.
7. D. E. Liddle, "The DIGIVUE Display/Memory Unit: A New Display System Technology," Owens-Illinois Electro/Optical Display Development Technical Bulletin DU-140, July 1, 1971.
8. ARPA Contract DAAB07-70-C-0243, U.S. Army Elect Command, Fort Monmouth.
9. J. Stifle, "A Plasma Display Terminal," CERL Report X-15, March, 1970.

10. R. L. Johnson, "Final Report, Rome Air Development Center Contract for Research on Data Manipulation and Sensing in the Plasma Display," Contract #F30602-70-C-0145.
11. H. J. Hoehn and R. A. Martel, "A 60 Line per Inch Plasma Display Panel," *IEEE Trans. on Electron Devices*, Vol. ED-18, #9, September, 1971, pp. 659-663.
12. R. L. Johnson, "The Device Characteristics of the Plasma Display Element," *IEEE Trans. on Electron Devices*, Vol. ED-18, #9, September, 1971, pp. 642-649.



UNIVERSITY OF ILLINOIS-URBANA

510.841L63C C001
CAC DOCUMENT\$URBANA
21-30 1971-72



3 0112 007263988